\*\*\* Running vivado

with args -log State\_Machine.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source State\_Machine.tcl -notrace

\*\*\*\*\*\* Vivado v2017.4 (64-bit)

\*\*\*\* SW Build 2086221 on Fri Dec 15 20:55:39 MST 2017

\*\*\*\* IP Build 2085800 on Fri Dec 15 22:25:07 MST 2017

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source State\_Machine.tcl -notrace

Command: link\_design -top State\_Machine -part xc7z020clg484-1

Design is defaulting to srcset: sources\_1

Design is defaulting to constrset: constrs\_1

INFO: [Netlist 29-17] Analyzing 12 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2017.4

INFO: [Device 21-403] Loading part xc7z020clg484-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Parsing XDC File [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc]

WARNING: [Vivado 12-584] No ports matched 'oled\_dc'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:40]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:40]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'oled\_res'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:41]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:41]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'oled\_sclk'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:42]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:42]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'oled\_sdin'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:43]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:43]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'oled\_vbat'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:44]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:44]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'oled\_vdd'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:45]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:45]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'hdmi\_cec'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:49]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:49]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'hdmi\_clk\_n'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:50]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:50]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'hdmi\_clk\_p'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:51]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:51]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'hdmi\_d\_n[0]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:52]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:52]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'hdmi\_d\_p[0]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:53]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:53]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'hdmi\_d\_n[1]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:54]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:54]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'hdmi\_d\_p[1]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:55]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:55]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'hdmi\_d\_n[2]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:56]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:56]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'hdmi\_d\_p[2]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:57]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:57]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'hdmi\_hpd'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:58]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:58]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'hdmi\_out\_en'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:59]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:59]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'hdmi\_scl'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:60]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:60]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'hdmi\_sda'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:61]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:61]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'vga\_b[0]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:65]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:65]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'vga\_b[1]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:66]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:66]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'vga\_b[2]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:67]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:67]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'vga\_b[3]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:68]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:68]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'vga\_b[4]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:69]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:69]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'vga\_g[0]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:70]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:70]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'vga\_g[1]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:71]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:71]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'vga\_g[2]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:72]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:72]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'vga\_g[3]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:73]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:73]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'vga\_g[4]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:74]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:74]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'vga\_g[5]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:75]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:75]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'vga\_hs'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:76]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:76]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'vga\_r[0]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:77]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:77]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'vga\_r[1]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:78]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:78]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'vga\_r[2]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:79]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:79]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'vga\_r[3]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:80]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:80]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'vga\_r[4]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:81]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:81]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'vga\_vs'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:82]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:82]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'ac\_bclk'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:86]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:86]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'ac\_mclk'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:87]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:87]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'ac\_muten'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:88]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:88]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'ac\_pbdat'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:89]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:89]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'ac\_pblrc'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:90]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:90]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'ac\_recdat'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:91]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:91]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'ac\_reclrc'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:92]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:92]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'ac\_scl'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:93]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:93]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'ac\_sda'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:94]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:94]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'ps2\_clk[0]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:98]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:98]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'ps2\_clk[1]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:99]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:99]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'ps2\_data[0]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:100]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:100]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'ps2\_data[1]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:101]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:101]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'uart\_rxd\_out'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:105]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:105]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'uart\_txd\_in'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:106]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:106]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'sseg\_an[0]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:110]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:110]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'sseg\_an[1]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:111]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:111]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'sseg\_an[2]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:112]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:112]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'sseg\_an[3]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:113]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:113]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'sseg\_ca'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:114]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:114]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'sseg\_cb'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:115]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:115]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'sseg\_cc'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:116]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:116]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'sseg\_cd'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:117]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:117]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'sseg\_ce'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:118]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:118]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'sseg\_cf'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:119]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:119]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'sseg\_cg'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:120]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:120]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'sseg\_dp'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:121]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:121]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_b[0]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:125]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:125]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_b[1]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:126]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:126]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_b[2]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:127]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:127]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_b[3]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:128]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:128]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_b[4]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:129]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:129]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_b[5]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:130]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:130]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_b[6]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:131]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:131]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_b[7]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:132]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:132]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_dclk'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:133]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:133]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_de'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:134]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:134]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_disp'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:135]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:135]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_g[0]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:136]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:136]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_g[1]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:137]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:137]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_g[2]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:138]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:138]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_g[3]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:139]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:139]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_g[4]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:140]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:140]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_g[5]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:141]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:141]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_g[6]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:142]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:142]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_g[7]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:143]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:143]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_hs'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:144]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:144]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_r[0]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:145]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:145]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_r[1]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:146]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:146]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_r[2]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:147]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:147]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_r[3]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:148]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:148]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_r[4]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:149]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:149]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_r[5]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:150]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:150]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_r[6]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:151]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:151]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_r[7]'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:152]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:152]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tft\_vs'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:153]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:153]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tp\_irq'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:154]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:154]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tp\_res'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:155]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:155]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tp\_sck'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:156]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:156]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'tp\_sda'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:157]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:157]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'bck\_dim'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:161]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:161]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'adc\_cs'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:165]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:165]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'adc\_sclk'. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:166]

INFO: [Common 17-14] Message 'Vivado 12-584' appears 100 times and further instances of the messages will be disabled. Use the Tcl command set\_msg\_config to change the current settings. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:166]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:166]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

INFO: [Common 17-14] Message 'Common 17-55' appears 100 times and further instances of the messages will be disabled. Use the Tcl command set\_msg\_config to change the current settings. [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc:166]

Finished Parsing XDC File [C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.srcs/constrs\_1/new/Master\_ICD.xdc]

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

9 Infos, 100 Warnings, 100 Critical Warnings and 0 Errors encountered.

link\_design completed successfully

link\_design: Time (s): cpu = 00:00:08 ; elapsed = 00:00:08 . Memory (MB): peak = 617.340 ; gain = 334.859

Command: opt\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7z020'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7z020'

Running DRC as a precondition to command opt\_design

Starting DRC Task

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Project 1-461] DRC finished with 0 Errors

INFO: [Project 1-462] Please refer to the DRC report (report\_drc) for more information.

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.522 . Memory (MB): peak = 632.117 ; gain = 14.777

INFO: [Timing 38-35] Done setting XDC timing constraints.

Starting Logic Optimization Task

Phase 1 Retarget

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Opt 31-49] Retargeted 0 cell(s).

Phase 1 Retarget | Checksum: 1d0726a03

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.012 . Memory (MB): peak = 1187.469 ; gain = 0.000

INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Phase 2 Constant propagation | Checksum: 1d0726a03

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.015 . Memory (MB): peak = 1187.469 ; gain = 0.000

INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep

Phase 3 Sweep | Checksum: 1d0726a03

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.017 . Memory (MB): peak = 1187.469 ; gain = 0.000

INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization

Phase 4 BUFG optimization | Checksum: 1d0726a03

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.021 . Memory (MB): peak = 1187.469 ; gain = 0.000

INFO: [Opt 31-389] Phase BUFG optimization created 0 cells and removed 0 cells

Phase 5 Shift Register Optimization

Phase 5 Shift Register Optimization | Checksum: 1d0726a03

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.022 . Memory (MB): peak = 1187.469 ; gain = 0.000

INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 1187.469 ; gain = 0.000

Ending Logic Optimization Task | Checksum: 1d0726a03

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.024 . Memory (MB): peak = 1187.469 ; gain = 0.000

Starting Power Optimization Task

INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.

Ending Power Optimization Task | Checksum: 1d0726a03

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.006 . Memory (MB): peak = 1187.469 ; gain = 0.000

INFO: [Common 17-83] Releasing license: Implementation

24 Infos, 100 Warnings, 100 Critical Warnings and 0 Errors encountered.

opt\_design completed successfully

opt\_design: Time (s): cpu = 00:00:11 ; elapsed = 00:00:11 . Memory (MB): peak = 1187.469 ; gain = 570.129

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.075 . Memory (MB): peak = 1187.469 ; gain = 0.000

INFO: [Common 17-1381] The checkpoint 'C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.runs/impl\_2/State\_Machine\_opt.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file State\_Machine\_drc\_opted.rpt -pb State\_Machine\_drc\_opted.pb -rpx State\_Machine\_drc\_opted.rpx

Command: report\_drc -file State\_Machine\_drc\_opted.rpt -pb State\_Machine\_drc\_opted.pb -rpx State\_Machine\_drc\_opted.rpx

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2017.4/data/ip'.

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Coretcl 2-168] The results of DRC are in file C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.runs/impl\_2/State\_Machine\_drc\_opted.rpt.

report\_drc completed successfully

INFO: [Chipscope 16-241] No debug cores found in the current design.

Before running the implement\_debug\_core command, either use the Set Up Debug wizard (GUI mode)

or use the create\_debug\_core and connect\_debug\_core Tcl commands to insert debug cores into the design.

Command: place\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7z020'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7z020'

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Running DRC as a precondition to command place\_design

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Placer Task

INFO: [Place 30-611] Multithreading enabled for place\_design using a maximum of 2 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1187.469 ; gain = 0.000

Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 185ca470b

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.003 . Memory (MB): peak = 1187.469 ; gain = 0.000

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1187.469 ; gain = 0.000

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

INFO: [Timing 38-35] Done setting XDC timing constraints.

WARNING: [Place 30-574] Poor placement for routing between an IO pin and BUFG. This is normally an ERROR but the CLOCK\_DEDICATED\_ROUTE constraint is set to FALSE allowing your design to continue. The use of this override is highly discouraged as it may lead to very poor timing results. It is recommended that this error condition be corrected in the design.

Clock\_IBUF\_inst (IBUF.O) is locked to IOB\_X0Y42

Clock\_IBUF\_BUFG\_inst (BUFG.I) is provisionally placed by clockplacer on BUFGCTRL\_X0Y0

Resolution: Poor placement of an IO pin and a BUFG has resulted in the router using a non-dedicated path between the two. There are several things that could trigger this DRC, each of which can cause unpredictable clock insertion delays that result in poor timing. This DRC could be caused by any of the following: (a) a clock port was placed on a pin that is not a CCIO-pin (b)the BUFG has not been placed in the same half of the device or SLR as the CCIO-pin (c) a single ended clock has been placed on the N-Side of a differential pair CCIO-pin.

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: 1e410181f

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.904 . Memory (MB): peak = 1187.469 ; gain = 0.000

Phase 1.3 Build Placer Netlist Model

Phase 1.3 Build Placer Netlist Model | Checksum: 20dff3fb2

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.939 . Memory (MB): peak = 1187.469 ; gain = 0.000

Phase 1.4 Constrain Clocks/Macros

Phase 1.4 Constrain Clocks/Macros | Checksum: 20dff3fb2

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.942 . Memory (MB): peak = 1187.469 ; gain = 0.000

Phase 1 Placer Initialization | Checksum: 20dff3fb2

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.943 . Memory (MB): peak = 1187.469 ; gain = 0.000

Phase 2 Global Placement

Phase 2 Global Placement | Checksum: 25f647fb9

Time (s): cpu = 00:00:02 ; elapsed = 00:00:01 . Memory (MB): peak = 1187.469 ; gain = 0.000

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros

Phase 3.1 Commit Multi Column Macros | Checksum: 25f647fb9

Time (s): cpu = 00:00:02 ; elapsed = 00:00:01 . Memory (MB): peak = 1187.469 ; gain = 0.000

Phase 3.2 Commit Most Macros & LUTRAMs

Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 1e7a5c8d2

Time (s): cpu = 00:00:02 ; elapsed = 00:00:01 . Memory (MB): peak = 1187.469 ; gain = 0.000

Phase 3.3 Area Swap Optimization

Phase 3.3 Area Swap Optimization | Checksum: 28ad837ed

Time (s): cpu = 00:00:02 ; elapsed = 00:00:01 . Memory (MB): peak = 1187.469 ; gain = 0.000

Phase 3.4 Pipeline Register Optimization

Phase 3.4 Pipeline Register Optimization | Checksum: 28ad837ed

Time (s): cpu = 00:00:02 ; elapsed = 00:00:01 . Memory (MB): peak = 1187.469 ; gain = 0.000

Phase 3.5 Small Shape Detail Placement

Phase 3.5 Small Shape Detail Placement | Checksum: 1d5ae715c

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 1187.469 ; gain = 0.000

Phase 3.6 Re-assign LUT pins

Phase 3.6 Re-assign LUT pins | Checksum: 1d5ae715c

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 1187.469 ; gain = 0.000

Phase 3.7 Pipeline Register Optimization

Phase 3.7 Pipeline Register Optimization | Checksum: 1d5ae715c

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 1187.469 ; gain = 0.000

Phase 3 Detail Placement | Checksum: 1d5ae715c

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 1187.469 ; gain = 0.000

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization

Phase 4.1 Post Commit Optimization | Checksum: 1d5ae715c

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 1187.469 ; gain = 0.000

Phase 4.2 Post Placement Cleanup

Phase 4.2 Post Placement Cleanup | Checksum: 1d5ae715c

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 1187.469 ; gain = 0.000

Phase 4.3 Placer Reporting

Phase 4.3 Placer Reporting | Checksum: 1d5ae715c

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 1187.469 ; gain = 0.000

Phase 4.4 Final Placement Cleanup

Phase 4.4 Final Placement Cleanup | Checksum: 1bb441270

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 1187.469 ; gain = 0.000

Phase 4 Post Placement Optimization and Clean-Up | Checksum: 1bb441270

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 1187.469 ; gain = 0.000

Ending Placer Task | Checksum: 1638b5660

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 1187.469 ; gain = 0.000

INFO: [Common 17-83] Releasing license: Implementation

42 Infos, 101 Warnings, 100 Critical Warnings and 0 Errors encountered.

place\_design completed successfully

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.059 . Memory (MB): peak = 1187.469 ; gain = 0.000

INFO: [Common 17-1381] The checkpoint 'C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.runs/impl\_2/State\_Machine\_placed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_io -file State\_Machine\_io\_placed.rpt

report\_io: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.083 . Memory (MB): peak = 1187.469 ; gain = 0.000

INFO: [runtcl-4] Executing : report\_utilization -file State\_Machine\_utilization\_placed.rpt -pb State\_Machine\_utilization\_placed.pb

report\_utilization: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.055 . Memory (MB): peak = 1187.469 ; gain = 0.000

INFO: [runtcl-4] Executing : report\_control\_sets -verbose -file State\_Machine\_control\_sets\_placed.rpt

report\_control\_sets: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.006 . Memory (MB): peak = 1187.469 ; gain = 0.000

Command: route\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7z020'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7z020'

Running DRC as a precondition to command route\_design

INFO: [DRC 23-27] Running DRC with 2 threads

WARNING: [DRC PLCK-12] Clock Placer Checks: Poor placement for routing between an IO pin and BUFG.

Resolution: Poor placement of an IO pin and a BUFG has resulted in the router using a non-dedicated path between the two. There are several things that could trigger this DRC, each of which can cause unpredictable clock insertion delays that result in poor timing. This DRC could be caused by any of the following: (a) a clock port was placed on a pin that is not a CCIO-pin (b)the BUFG has not been placed in the same half of the device or SLR as the CCIO-pin (c) a single ended clock has been placed on the N-Side of a differential pair CCIO-pin.

This is normally an ERROR but the CLOCK\_DEDICATED\_ROUTE constraint is set to FALSE allowing your design to continue. The use of this override is highly discouraged as it may lead to very poor timing results. It is recommended that this error condition be corrected in the design.

Clock\_IBUF\_inst (IBUF.O) is locked to IOB\_X0Y42

Clock\_IBUF\_BUFG\_inst (BUFG.I) is provisionally placed by clockplacer on BUFGCTRL\_X0Y0

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors, 1 Warnings

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Routing Task

INFO: [Route 35-254] Multithreading enabled for route\_design using a maximum of 2 CPUs

Checksum: PlaceDB: 876efcf3 ConstDB: 0 ShapeSum: dc1c596d RouteDB: 0

Phase 1 Build RT Design

Phase 1 Build RT Design | Checksum: bf4d1504

Time (s): cpu = 00:00:28 ; elapsed = 00:00:25 . Memory (MB): peak = 1325.219 ; gain = 137.750

Post Restoration Checksum: NetGraph: 9ac2264c NumContArr: 248aeeb8 Constraints: 0 Timing: 0

Phase 2 Router Initialization

INFO: [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.

Phase 2.1 Fix Topology Constraints

Phase 2.1 Fix Topology Constraints | Checksum: bf4d1504

Time (s): cpu = 00:00:28 ; elapsed = 00:00:25 . Memory (MB): peak = 1331.391 ; gain = 143.922

Phase 2.2 Pre Route Cleanup

Phase 2.2 Pre Route Cleanup | Checksum: bf4d1504

Time (s): cpu = 00:00:28 ; elapsed = 00:00:25 . Memory (MB): peak = 1331.391 ; gain = 143.922

Number of Nodes with overlaps = 0

Phase 2 Router Initialization | Checksum: df91fa40

Time (s): cpu = 00:00:28 ; elapsed = 00:00:25 . Memory (MB): peak = 1340.828 ; gain = 153.359

Phase 3 Initial Routing

Phase 3 Initial Routing | Checksum: bb35e3da

Time (s): cpu = 00:00:29 ; elapsed = 00:00:25 . Memory (MB): peak = 1340.828 ; gain = 153.359

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0

Number of Nodes with overlaps = 4

Number of Nodes with overlaps = 0

Phase 4.1 Global Iteration 0 | Checksum: ea4401ee

Time (s): cpu = 00:00:29 ; elapsed = 00:00:25 . Memory (MB): peak = 1340.828 ; gain = 153.359

Phase 4 Rip-up And Reroute | Checksum: ea4401ee

Time (s): cpu = 00:00:29 ; elapsed = 00:00:25 . Memory (MB): peak = 1340.828 ; gain = 153.359

Phase 5 Delay and Skew Optimization

Phase 5 Delay and Skew Optimization | Checksum: ea4401ee

Time (s): cpu = 00:00:29 ; elapsed = 00:00:25 . Memory (MB): peak = 1340.828 ; gain = 153.359

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter

Phase 6.1 Hold Fix Iter | Checksum: ea4401ee

Time (s): cpu = 00:00:29 ; elapsed = 00:00:25 . Memory (MB): peak = 1340.828 ; gain = 153.359

Phase 6 Post Hold Fix | Checksum: ea4401ee

Time (s): cpu = 00:00:29 ; elapsed = 00:00:25 . Memory (MB): peak = 1340.828 ; gain = 153.359

Phase 7 Route finalize

Router Utilization Summary

Global Vertical Routing Utilization = 0.0201926 %

Global Horizontal Routing Utilization = 0.0106491 %

Routable Net Status\*

\*Does not include unroutable nets such as driverless and loadless.

Run report\_route\_status for detailed report.

Number of Failed Nets = 0

Number of Unrouted Nets = 0

Number of Partially Routed Nets = 0

Number of Node Overlaps = 0

Utilization threshold used for congestion level computation: 0.85

Congestion Report

North Dir 1x1 Area, Max Cong = 11.7117%, No Congested Regions.

South Dir 1x1 Area, Max Cong = 14.4144%, No Congested Regions.

East Dir 1x1 Area, Max Cong = 11.7647%, No Congested Regions.

West Dir 1x1 Area, Max Cong = 10.2941%, No Congested Regions.

Phase 7 Route finalize | Checksum: ea4401ee

Time (s): cpu = 00:00:29 ; elapsed = 00:00:25 . Memory (MB): peak = 1340.828 ; gain = 153.359

Phase 8 Verifying routed nets

Verification completed successfully

Phase 8 Verifying routed nets | Checksum: ea4401ee

Time (s): cpu = 00:00:29 ; elapsed = 00:00:25 . Memory (MB): peak = 1340.828 ; gain = 153.359

Phase 9 Depositing Routes

Phase 9 Depositing Routes | Checksum: ba3f93bf

Time (s): cpu = 00:00:29 ; elapsed = 00:00:25 . Memory (MB): peak = 1340.828 ; gain = 153.359

INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:29 ; elapsed = 00:00:25 . Memory (MB): peak = 1340.828 ; gain = 153.359

Routing Is Done.

INFO: [Common 17-83] Releasing license: Implementation

54 Infos, 102 Warnings, 100 Critical Warnings and 0 Errors encountered.

route\_design completed successfully

route\_design: Time (s): cpu = 00:00:30 ; elapsed = 00:00:26 . Memory (MB): peak = 1340.828 ; gain = 153.359

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.064 . Memory (MB): peak = 1340.828 ; gain = 0.000

INFO: [Common 17-1381] The checkpoint 'C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.runs/impl\_2/State\_Machine\_routed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file State\_Machine\_drc\_routed.rpt -pb State\_Machine\_drc\_routed.pb -rpx State\_Machine\_drc\_routed.rpx

Command: report\_drc -file State\_Machine\_drc\_routed.rpt -pb State\_Machine\_drc\_routed.pb -rpx State\_Machine\_drc\_routed.rpx

INFO: [IP\_Flow 19-1839] IP Catalog is up to date.

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Coretcl 2-168] The results of DRC are in file C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.runs/impl\_2/State\_Machine\_drc\_routed.rpt.

report\_drc completed successfully

INFO: [runtcl-4] Executing : report\_methodology -file State\_Machine\_methodology\_drc\_routed.rpt -pb State\_Machine\_methodology\_drc\_routed.pb -rpx State\_Machine\_methodology\_drc\_routed.rpx

Command: report\_methodology -file State\_Machine\_methodology\_drc\_routed.rpt -pb State\_Machine\_methodology\_drc\_routed.pb -rpx State\_Machine\_methodology\_drc\_routed.rpx

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [DRC 23-133] Running Methodology with 2 threads

INFO: [Coretcl 2-1520] The results of Report Methodology are in file C:/Users/FrankCf/Desktop/Integrated Circuit Coursework/project\_1/project\_1.runs/impl\_2/State\_Machine\_methodology\_drc\_routed.rpt.

report\_methodology completed successfully

INFO: [runtcl-4] Executing : report\_power -file State\_Machine\_power\_routed.rpt -pb State\_Machine\_power\_summary\_routed.pb -rpx State\_Machine\_power\_routed.rpx

Command: report\_power -file State\_Machine\_power\_routed.rpt -pb State\_Machine\_power\_summary\_routed.pb -rpx State\_Machine\_power\_routed.rpx

WARNING: [Power 33-232] No user defined clocks were found in the design!

Resolution: Please specify clocks using create\_clock/create\_generated\_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate

INFO: [Timing 38-35] Done setting XDC timing constraints.

Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation

66 Infos, 103 Warnings, 100 Critical Warnings and 0 Errors encountered.

report\_power completed successfully

INFO: [runtcl-4] Executing : report\_route\_status -file State\_Machine\_route\_status.rpt -pb State\_Machine\_route\_status.pb

INFO: [runtcl-4] Executing : report\_timing\_summary -max\_paths 10 -file State\_Machine\_timing\_summary\_routed.rpt -rpx State\_Machine\_timing\_summary\_routed.rpx -warn\_on\_violation

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs

WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.

INFO: [runtcl-4] Executing : report\_incremental\_reuse -file State\_Machine\_incremental\_reuse\_routed.rpt

INFO: [Vivado\_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.

INFO: [runtcl-4] Executing : report\_clock\_utilization -file State\_Machine\_clock\_utilization\_routed.rpt

Command: write\_bitstream -force State\_Machine.bit

Attempting to get a license for feature 'Implementation' and/or device 'xc7z020'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7z020'

Running DRC as a precondition to command write\_bitstream

INFO: [IP\_Flow 19-1839] IP Catalog is up to date.

INFO: [DRC 23-27] Running DRC with 2 threads

WARNING: [DRC PDRC-153] Gated clock check: Net GuessLED\_reg\_i\_1\_n\_0 is a gated clock net sourced by a combinational pin GuessLED\_reg\_i\_1/O, cell GuessLED\_reg\_i\_1. This is not good design practice and will likely impact performance. For SLICE registers, for example, use the CE pin to control the loading of data.

WARNING: [DRC PDRC-153] Gated clock check: Net Next\_State is a gated clock net sourced by a combinational pin FSM\_onehot\_Next\_State\_reg[6]\_i\_2/O, cell FSM\_onehot\_Next\_State\_reg[6]\_i\_2. This is not good design practice and will likely impact performance. For SLICE registers, for example, use the CE pin to control the loading of data.

WARNING: [DRC PDRC-153] Gated clock check: Net NumberLED\_reg[3]\_i\_2\_n\_0 is a gated clock net sourced by a combinational pin NumberLED\_reg[3]\_i\_2/O, cell NumberLED\_reg[3]\_i\_2. This is not good design practice and will likely impact performance. For SLICE registers, for example, use the CE pin to control the loading of data.

WARNING: [DRC PDRC-153] Gated clock check: Net WinLED\_reg\_i\_2\_n\_0 is a gated clock net sourced by a combinational pin WinLED\_reg\_i\_2/O, cell WinLED\_reg\_i\_2. This is not good design practice and will likely impact performance. For SLICE registers, for example, use the CE pin to control the loading of data.

WARNING: [DRC PDRC-153] Gated clock check: Net reset\_counter\_reg\_i\_1\_n\_0 is a gated clock net sourced by a combinational pin reset\_counter\_reg\_i\_1/O, cell reset\_counter\_reg\_i\_1. This is not good design practice and will likely impact performance. For SLICE registers, for example, use the CE pin to control the loading of data.

WARNING: [DRC ZPS7-1] PS7 block required: The PS7 cell must be used in this Zynq design in order to enable correct default configuration.

INFO: [Vivado 12-3199] DRC finished with 0 Errors, 6 Warnings

INFO: [Vivado 12-3200] Please refer to the DRC report (report\_drc) for more information.

INFO: [Project 1-821] Please set project.enableDesignId to be 'true'.

INFO: [Designutils 20-2272] Running write\_bitstream with 2 threads.

Loading data files...

Loading site data...

Loading route data...

Processing options...

Creating bitmap...

Creating bitstream...

Writing bitstream ./State\_Machine.bit...

INFO: [Vivado 12-1842] Bitgen Completed Successfully.

INFO: [Project 1-120] WebTalk data collection is mandatory when using a WebPACK part without a full Vivado license. To see the specific WebTalk data collected for your design, open the usage\_statistics\_webtalk.html or usage\_statistics\_webtalk.xml file in the implementation directory.

Access is denied.

Access is denied.

INFO: [Common 17-83] Releasing license: Implementation

83 Infos, 110 Warnings, 100 Critical Warnings and 0 Errors encountered.

write\_bitstream completed successfully

write\_bitstream: Time (s): cpu = 00:00:14 ; elapsed = 00:00:14 . Memory (MB): peak = 1798.418 ; gain = 424.645

INFO: [Common 17-206] Exiting Vivado at Wed Mar 27 17:00:51 2019...